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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

JUNG-KEUN AHN et al.

Serial No.:

10/698,433

Examiner:

LONEY DONALD J.

Filed:

3 November 2003

Art Unit:

1772

For:

PLASMA DISPLAY PANEL

# Information Disclosure Statement

Commissioner for Patents P.O.Box 1450 Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §1.56, and §§1.97 and 1.98 as amended, Applicant cites, describes, and provides copies of the following art references.

#### **FOREIGN PATENT REFERENCE:**

- Japanese Patent Publication No. 2001-307643 to Yoshikawa, et al., entitled DISPLAY PANEL AND FLAT DISPLAY DEVICE, published on 2 November 2001 (with English abstract).
- Japanese Patent Publication No. 2000-277020 to Tanaka, entitled PLASMA DISPLAY *PANEL*, published on 6 October 2000 (with English abstract).
- Japanese Patent Publication No. 2001-160360 to Saito, et al., entitled PLASMA DISPLAY PANEL, published on 12 June 2001 (with English abstract).(already cited in Information Disclosure Statement filed on 3 November 2003 and 8 December 2004).
- Japanese Patent Publication No. 2002-304948 to Morikawa, et al., entitled PLASMA DISPLAY PANEL, published on 18 October 2002 (with English abstract).

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- Japanese Patent Publication No. 2000-340123 to Amamiya, entitled PLASMA
   DISPLAY PANEL, published on 8 December 2000 (with English abstract).
- International Patent Publication No. 02/084689 to Fujinaga, *et al.*, entitled *PARTITION WALL FORMING METHOD FOR PLASMA DISPLAY PANELS USING SANDBLAST*, published on 24 October 2002 (with English abstract).

### **OTHER DOCUMENTS:**

Japanese Office action for Japanese Patent Application No. 2003-277532, issued on
 6 June 2006.

#### **DISCUSSION**

Yoshikawa JP'643, according to the Japanese Office action in applicant's Japanese patent application Serial No. 2003-277532, discloses that a display panel is equipped with a substrate, a barrier wall formed on the substrate and a dummy barrier wall. An effective region for a display and an ineffective region that is located at a peripheral portion of the effective region and surrounds the effective region, are comprised. For a part of the substrate corresponding to the effective region, plural numbers of the barrier walls of a stripe shape are formed, and the dummy barrier walls are formed on the part of the substrate positioned between the connecting portion of the ineffective region connecting with an interior space of a flat display device in assembling the flat display device and the effective region.

Tanaka JP'020, discloses that a front glass substrate and a back glass substrate are arranged opposite to each other through a discharge space. Peripheral part thereof is sealed by a seal layer. A first barrier for partitioning the discharge space of a display area is formed. A second barrier extended in nearly parallel with the seal layer and having plural intermittent parts (notch part, interval) is formed in an area inside of the seal layer and outside of the display area. A third barrier is formed in nearly parallel with the seal layer at a position opposite to the intermittent part of the second barrier in an area outside of the display area. Diffusion of the impurity gas discharged from

the seal layer into the display area is prevented, and pollution of the surface of a protecting film is prevented.

Morikawa JP'948, discloses that this plasma display panel is equipped with a back substrate, plural discharge cells formed by arranging them in a zigzag shape on the back substrate, plural barrier ribs surrounding respective discharge spaces of the plural discharge cells, a phosphor film formed on the inner wall surface of each barrier rib and on the back substrate inside the barrier plate, and a front substrate disposed face to face with the back substrate while having a discharge electrode corresponding to the discharge cell. The barrier rib is formed separately from other adjacent barrier ribs surrounding the discharge cells, and its outline on a plan view is formed in a polygonal shape with number of sides more than that of a pentagon.

Amamiya JP'123, discloses that this plasma display panel is provided with barrier ribs disposed between a front glass substrate and a back glass substrate and dividing a discharge space in the row direction and in the column direction into unit luminous areas by longitudinal ribs extending in the column direction and by lateral ribs extending in the row direction. Raised parts are formed on portions of dielectric layers confronting the lateral ribs of the barrier ribs so as to project toward the lateral ribs side to close a space left by the lateral ribs, and outer end parts of the barrier ribs are positioned in positions opposite to portions of the dielectric layers where no raised parts are formed.

Fujinaga WO'689, discloses that a partition wall is formed by the steps of preparing a laminar partition wall material covering the display region and outer side of a substrate surface, preparing a patterning mask extending across the display region and outer side, making the portion disposed outside the display region in the mask into a lattice-like pattern, patterning the partition wall material locally covered by the mask by means of sand blast, and firing the patterned partition wall material.

PATENT P56975

Pursuant to 37 CFR §1.97(d), the undersigned attorney hereby certifies that each item of

information contained in this Information Disclosure Statement was cited in a communication from

a foreign patent office in a counterpart foreign patent application not more than three (3) months

prior to the filing of the statement.

The citation of the foregoing references is not intended to constitute an assertion that other

or more relevant art does not exist. Accordingly, the Examiner is requested to make a wide-ranging

and thorough search of the relevant art.

Pursuant to 37 C.F.R. §1.97(c)(2), the fee set forth under 37 C.F.R.§1.17(p) of \$180.00

accompanies this Information Disclosure Statement. Should the check become lost, be deficient in

payment, or should other fees be incurred, the Commissioner is authorized to charge Deposit

Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

Respectfully submitted,

Robert E. Bushnell

Reg. No.: 27,774

Attorney for the Applicant

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Folio: P56975 Date: 6/27/06

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# INFORMATION DISCLOSE RE STATEMENT

PTO-1449 (PAGE 1 OF 1)

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APPLICANT JUNG-KEUN AH	IN et al.
FILING DATE 3 November 2003	GROUP 1772

			U.S. PATENT DOCUMENTS							
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<u>.</u>	JP 2001-307643	11/01	JAPAN			Abstract				
	JP 2000-277020	10/00	JAPAN			Abstract				
	JP 2002-304948	10/02	JAPAN			Abstract				
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Japanese Office Action of the Japanese Patent Application No. 2003-277532, issued on 6 June 2006										
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